Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended) An output buffer, comprising:

a first circuit coupled between a first power line and a pad; and

a second circuit coupled between a second power line and the pad, the second circuit comprising:

a resistor constructed by a well region of a second conductivity type ~~deposited~~ disposed on a substrate of a first conductivity type, the resistor comprising ~~a first end and a second end~~ a fourth doped region of the second conductivity type and a fifth doped region of the second conductivity type, the ~~first end~~ fourth doped region being ~~a doped region of the second conductivity type at least partially overlapping the well region and~~ coupled to the pad; and

a first doped region of the first conductivity type~~, electrically floated~~ ~~in~~ disposed within the well region, wherein the first doped region is electrically floated and spaced apart from the fourth doped region; and

an electrostatic discharge protection component, coupled between the ~~second end~~ fifth doped region and the second power line.

Claim 2 (currently amended) An output buffer, comprising:

a first circuit coupled between a first power line and a pad; and

a second circuit coupled between a second power line and the pad, the

second circuit comprising:

a resistor constructed by a well region of a second conductivity type ~~deposited~~ disposed on a substrate of a first conductivity type, the resistor comprising a first end and a second end, the first end being a doped region of the second conductivity type at least partially overlapping the well region and coupled to the pad;

a first doped region of the first conductivity type[[,]] disposed [[in]] within the well region;

a capacitor coupled between the pad and the first doped region; and

an electrostatic discharge protection component, coupled between the second end and the second power line.

Claim 3 (currently amended) The output buffer of claim 1, wherein the electrostatic discharge protection element is a MOS transistor comprising a gate, a drain and a source, the drain being coupled to the ~~second end of the resistor~~ fifth doped region and the source being coupled to the second power line.

Claim 4 (currently amended) The output buffer of claim 3, wherein the drain ~~and the source are respectively comprised of~~ is a second doped region of the second conductivity type, and the source is a third doped region of the second conductivity type.

Claims 5-7 (withdrawn).

Claim 8-10 (cancelled).

Claims 11-12 (withdrawn).

Claim 13 (cancelled).

Claim 14 (currently amended) The output buffer of claim 1, wherein the substrate is coupled to the second power line through a sixth doped region of the first conductivity type.

Claims 15-30 (withdrawn).

Claim 31 (cancelled).

Claims 32-33 (withdrawn).

Claim 34 (currently amended) An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first ~~conductive~~ conductivity type;

a first doped region and a second doped region of a second ~~conductive~~ conductivity type formed in the substrate, the first doped region and the second doped region being spaced apart enabling a channel region formed in between;

a well region of the second ~~conductive~~ conductivity type, formed in the substrate; and

a fourth doped region and a fifth doped region of the second conductivity type formed in the well region, the fourth doped region coupled to the first node; and

a third doped region of the first ~~conductive~~ conductivity type disposed

[[in]] within the well region~~,and electrically floated in the well region so that the third doped region has no DC connection to the first node,~~ wherein the third doped region is electrically floated and is spaced apart from the fourth doped region, the first node is electrically coupled to the first doped region ~~and the well region~~ through the fourth doped region, the well region, and the fifth doped region, and the second node is electrically coupled to the second doped region.

Claim 35~37 (cancelled).

Claim 38 (currently amended) An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first ~~conductive~~ conductivity type;

a first doped region and a second doped region of a second ~~conductive~~ conductivity type formed in the substrate, the first and second doped regions being spaced apart enabling a channel formed in between;

~~a well region of the second conductive type, formed in the substrate; and~~

a resistor constructed by a well region of a second conductivity type being disposed on the substrate, the resistor comprising a fourth doped region and a fifth doped region of the second conductivity type; the fourth doped region coupled to the first node; and

a third doped region of the first ~~conductive~~ conductivity type disposed [[in]] within the well region, wherein the third doped region is coupled to the first node through a capacitor; the third doped region is spaced apart from the fourth doped region; the first node is electrically coupled to the first doped region [[and]] through the fourth doped region, the well region, and the

fifth doped region; and the second node is electrically coupled to the second doped region.

Claim 39 (currently amended) An output butter, comprising:

a first circuit coupled between a first power line and a pad; and

a second circuit coupled between a second power line and the pad, the second circuit comprising:

~~a resistor constructed by~~ a well region of a second ~~conductive~~ conductivity type disposed on a substrate of a first ~~conductive~~ conductivity type, ~~the resistor comprising a first end and a second end, the first end being a doped region of a second conductive type at least partially overlapping the well region and coupled to the pad~~;

a second doped region and a third doped region of a second conductivity type disposed in the well region, the second doped region being coupled to the pad;

a first doped region of the first conductivity type ~~deposed~~ disposed [[in]] within the well region, wherein ~~the first doped region is at least capacitively coupled the pad and electrically floated in the well region in that~~ the second doped region is spaced apart from the first doped region, there is no DC connection between the first doped region and the pad; and

an electrostatic discharge protection component coupled between the ~~second end~~ third doped region and the second power line.

Claim 40 (NEW) The output buffer of claim 1, wherein the first doped region is electrically floating between the fourth doped region and the fifth doped region.

Claim 41 (NEW) The output buffer of claim 1, wherein the first doped region is spaced apart from the fifth doped region.

Claim 42 (NEW) The output buffer of claim 1, wherein the fifth doped region is at least partially overlapping with the well region.

Claim 43 (NEW) The electrostatic discharge protection circuit of claim 34, wherein the third doped region is electrically floating between the fourth doped region and the fifth doped region.

Claim 44 (NEW) The electrostatic discharge protection circuit of claim 34, wherein the third doped region is spaced apart from the fifth doped region.

Claim 45 (NEW) The electrostatic discharge protection circuit of claim 34, wherein the fifth doped region is at least partially overlapping with the well region.

Claim 46 (NEW) The electrostatic discharge protection circuit of claim 38, wherein the third doped region is disposed between the fourth doped region and the fifth doped region.

Claim 47 (NEW) The electrostatic discharge protection circuit of claim 38, wherein the third doped region is spaced apart from the fifth doped region.

Claim 48 (NEW) The output buffer of claim 39, wherein the first doped

region is disposed between the second doped region and the third doped region.

Claim 49 (NEW) The output buffer of claim 39, wherein the first doped region is spaced apart from the third doped region.

Claim 50 (NEW) The output buffer of claim 39, wherein the first doped region is not directly connected to the pad.

Claim 51 (NEW) The output buffer of claim 39, wherein the first doped region is not connected to the pad.

Claim 52(NEW) An output butter, comprising:

a first circuit coupled between a first power line and a pad; and

a second circuit coupled between a second power line and the pad, the second circuit comprising:

a well region of a second conductivity type disposed on a substrate of a first conductivity type;

a first doped region and a second doped region of a second conductivity type disposed in the well region, the first doped region being coupled to the pad;

a third doped region of the first conductivity type disposed within the well region, wherein the third doped region is spaced apart from the first doped region, the first doped region is not electrically connected to the pad; and

an electrostatic discharge protection component coupled between the second doped region and the second power line.

Claim 53 (NEW) A semiconductor device, comprising:

a well region of a second conductivity type disposed on a substrate of a first conductivity type;

a first doped region of the second conductivity type disposed in the well region and coupled to a pad; and

a second doped region of the first conductivity type disposed within the well region, wherein the second doped region is electrically floated and space apart from the first doped region; and

an electrostatic discharge protection component, coupled between the well region and a first power line.

Claim 54 (NEW) The semiconductor device of claim 53, further comprising a third doped region of the second conductivity type disposed in the well region and coupled to the electrostatic discharge protection component.

Claim 55 (NEW) The semiconductor device of claim 54, wherein the second doped region is electrically floating between the first doped region and the third doped region.

Claim 56 (NEW) The semiconductor device of claim 54, wherein the second doped region is spaced apart from the third doped region.

Claim 57 (NEW) The semiconductor device of claim 54, wherein the third doped region is at least partially overlapping with the well region.

Claim 58 (NEW) The semiconductor device of claim 54, wherein the electrostatic discharge protection element is a MOS transistor comprising a gate, a drain and a source, the drain being coupled to the third doped region and the source being coupled to the first power line.

Claim 59 (NEW) The semiconductor device of claim 54, wherein the drain is a fourth doped region of the second conductivity type, and the source is a fifth doped region of the second conductivity type.

Claim 60 (NEW) A semiconductor device, comprising:

a well region of a second conductivity type disposed on a substrate of a first conductivity type;

a first doped region of the second conductivity type disposed in the well region and coupled to a pad;

a second doped region of the first conductivity type disposed within the well region, wherein the second doped region is electrically floated and space apart from the first doped region; and

a capacitor coupled between the pad and the second doped region and an electrostatic discharge protection component, coupled between the well region and a first power line.

Claim 61 (NEW) An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first conductivity type;

a first doped region and a second doped region of a second conductivity type formed in the substrate, the first doped region and the second doped region being spaced apart enabling a channel region formed in

between;

a well region of the second conductivity type formed in the substrate;

a third doped region of the second conductivity type formed in the well region and coupled to the first node; and

a fourth doped region of the first conductivity type disposed within the well region, wherein the fourth doped region is electrically floated and is spaced apart from the third doped region, the first node is electrically coupled to the first doped region through the third doped region and well region; and, the second node is electrically coupled to the second doped region.

Claim 62 (NEW) The electrostatic discharge protection circuit of claim 61, further comprising a fifth doped region of the second conductivity type disposed in the well region, wherein the fourth doped region is electrically floating between the third doped region and the fifth doped region.

Claim 63 (NEW) The electrostatic discharge protection circuit of claim 62, wherein the fourth doped region is spaced apart from the fifth doped region.

Claim 64 (NEW) The electrostatic discharge protection circuit of claim 62, wherein the fifth doped region is at least partially overlapping with the well region.

Claim 65 (NEW) An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first conductivity type;

a first doped region and a second doped region of a second conductivity type formed in the substrate, the first and second doped regions being spaced apart enabling a channel formed in between;

a well region of the second conductivity type formed in the substrate; and

a third doped region of the second conductivity type disposed in the well region and coupled to the first node;

a fourth doped region of the first conductivity type disposed within the well region, wherein the fourth doped region is coupled to the first node through a capacitor; wherein

the fourth doped region is spaced apart from the third doped region; the first node is electrically coupled to the first doped region through the third doped region and the well region; and the second node is electrically coupled to the second doped region.

Claim 66 (NEW) The electrostatic discharge protection circuit of claim 65, further comprising a fifth doped region of the second conductivity type disposed in the well region, and coupled to the second doped region.

Claim 67 (NEW) The electrostatic discharge protection circuit of claim 65, wherein the fourth doped region is disposed between the third doped region and the fifth doped region.

Claim 68 (NEW) The electrostatic discharge protection circuit of claim 65, wherein the fourth doped region is spaced apart from the fifth doped region.

Claim 69 (NEW) A semiconductor device, comprising:

a well region of a second conductivity type disposed on a substrate of a first conductivity type;

a first doped region of a second conductivity type disposed in the well region and coupled to a pad;

a second doped region of the first conductivity type disposed within the well region, wherein the second doped region is electrically coupled to the pad without direct connectivity to the pad; and

an electrostatic discharge protection component coupled between the well region and a first power line.

Claim 70 (NEW) The semiconductor device of claim 69, further comprising a third doped region of the second conductivity type disposed in the well region and coupled to the electrostatic discharge protection component.

Claim 71 (NEW) The semiconductor device of claim 69, wherein the second doped region is disposed between the first doped region and the third doped region.

Claim 72 (NEW) The semiconductor device of claim 69, wherein the second doped region is spaced apart from the third doped region.

Claim 73 (NEW) The output buffer of claim 69, wherein the electrostatic discharge protection element is a MOS transistor comprising a gate, a drain and a source, the drain being coupled to the third doped region and the source being coupled to the first power line.

Claim 74 (NEW) The semiconductor device of claim 69, wherein the drain is a fourth doped region of the second conductivity type, and the source is a fifth doped region of the second conductivity type.